REMARKS

Claims 11-20 are presently pending in the application. Claims 1-10 have been cancelled in the interest of expediting prosecution, and claims 11-20 have been added to assure Applicant the degree of protection to which his invention entitles him.

Claims 2-7 were rejected under 35 U.S.C. §112, second paragraph, due to purported problems of antecedents and unclear wording. Cancellation of these claims makes these rejections moot.

Claims 1-10 were rejected under 35 U.S.C. §102(b) as being anticipated by Ellis, U.S. Patent No. 5,606,491. Insofar as it may be deemed to apply to claims 11-20, this rejection is respectfully traversed.

THE CLAIMED INVENTION

The claimed invention is directed to a charge pump-type booster circuit. In an exemplary embodiment, the charge pump-type booster circuit includes a pair of input terminals 71, 72 for providing an input voltage; a charge capacitor 61; a first pair of switches 11, 12 capable of alternatively assuming a first condition, coupling the charge capacitor across the pair of input terminals to charge the charge capacitor to a voltage level substantially equal to the input voltage, and a second condition decoupling the charge capacitor from across the input terminals.

A second pair of switches 21, 22 is capable of assuming a first condition, coupling a first output capacitor 53 across a first serial combination, comprising the input terminals and the charge capacitor, to charge the first output capacitor to a voltage level substantially twice

the voltage level of the input voltage, and a second condition, decoupling the first output capacitor from the first serial combination,

A third pair of switches 31, 32 is capable of assuming a first condition, coupling a second output capacitor 51 across a second serial combination, comprising the charge capacitor and the first output capacitor, to charge the second output capacitor to a voltage level substantially three times the voltage level of the input voltage, and a second condition, decoupling the second output capacitor from the second serial combination.

A load 52, 54 can be in parallel with either the first output capacitor or the second output capacitor, or both, to receive voltage from such capacitors.

A more general exemplary embodiment includes a pair of input terminals for providing an input voltage; a charge capacitor; a pair of charge switches; N output capacitors, identified in sequence as output capacitor number 1 to output capacitor number N; and N pairs of boosting switches. The pair of charge switches is capable of alternatively assuming a first condition, coupling the charge capacitor across the pair of input terminals to charge the charge capacitor to a voltage level substantially equal to the voltage level of the input voltage, and a second condition decoupling the charge capacitor from across the input terminals.

A first one of the pairs of boosting switches is capable of alternatively assuming a first condition, coupling output capacitor number 1 across a first serial combination, comprising the input terminals and the charge capacitor, to charge output capacitor number 1 to a voltage level substantially twice the level of the input voltage, and a second condition decoupling output capacitor number 1 from the first serial combination.

A second one of the pairs of boosting switches is capable of alternatively assuming a

first condition, coupling output capacitor number 2 across a second serial combination, comprising the charge capacitor and output capacitor number 1, to charge output capacitor number 2 to a voltage level substantially three times the input voltage level, and a second condition decoupling output capacitor number 2 from the second serial combination.

Each of the remaining pairs of boosting switches is capable of assuming a first condition, coupling an associated output capacitor number n across an associated serial combination, comprising output capacitor number (n-2) and output capacitor number (n-1), to charge output capacitor number n to a voltage level at least equal to (n+1) times the input voltage level. N is an integer greater than 2, and n is an integer between 3 and N.

A load can be placed across any or all of the output capacitors to receive voltage from such capacitors.

In preferred embodiments, each switch comprises a thin film transistor.

THE ELLIS REFERENCE

Ellis discloses a multiplying and inverting charge pump circuit. A pair of input terminals 24, 25 provides an input voltage. A pair of switches 40, 44 is capable of alternatively assuming a first condition, coupling a charge capacitor 36 across the pair of input terminals to charge the charge capacitor to a voltage level substantially equal to the input voltage, and a second condition decoupling the charge capacitor from across the input terminals.

A set of three switches 42, 50, 54 is capable of assuming a first condition, coupling a booster capacitor 46 across a first serial combination, comprising the input terminals and the

charge capacitor, to charge the booster capacitor to a voltage level substantially twice the voltage level of the input voltage, and a second condition, decoupling the booster capacitor from the first serial combination.

Another pair of switches 52, 66 is capable of assuming a first condition, coupling an output capacitor 26 across a second serial combination, comprising the pair of input terminals and the booster capacitor, to charge the output capacitor to a voltage level substantially three times the voltage level of the input voltage, and a second condition, decoupling the output capacitor from the second serial combination.

Ellis discloses use of MOS transistors as the switches.

ARGUMENT

In Applicant's invention as set forth in, for example Figure 1 and claim 11, the second output capacitor is charged from the charge capacitor and the first output capacitor. In contrast in the charge pump circuit of Ellis, the output capacitor is charged from the input voltage and the booster capacitor. Consequently, Ellis utilizes more voltage from the input voltage source. In, for example, a mobile (cell) phone, this can drain the battery more rapidly. Thus, the claimed invention enables the cell phone to be used for a longer time between chargings.

In addition, Applicant's invention permits obtaining of N output voltages for application to N different loads. This is advantageous in, for example, a power supply for a display device which requires different voltage levels for different circuits. In contrast, in the Ellis charge pump circuit, as depicted in his Figures 1 and 2, only a single output voltage

level, three times the input voltage, can be obtained.

Further, in the claimed invention, each capacitor requires only a pair of switches to control charging of it to the desired voltage. Thus, in the exemplary embodiment of Figure 1 and claim 11, providing a load with an output voltage of a voltage level three times the voltage level of the input voltage requires six switches. With the Ellis circuit, in order to provide a load with an output voltage of a voltage level three times the voltage level of the input voltage requires seven switches.

As set forth in the specification at, for example, page 3, line 24 to page 4, line 2, MOS switches have a large size, and so when a charge pump circuit is constructed of MOS transistors, as in Ellis, the charge pump circuit has a large size. Use of thin film transistor switches reduces the size.

Whether using thin film transistor switches or MOS switches, it is desirable to minimize the number of switches required by the charge pump circuit. To achieve the same boost in voltage as in the claimed invention, Ellis requires an additional switch. Consequently, the claimed invention permits a smaller charge pump circuit for a given boost in voltage, whether the present invention is made of thin film transistor switches or other switches.

Claims 11-20 particularly point out and distinctly claim Applicant's invention in a manner distinguishing over Ellis. Accordingly, it is submitted that claims 11-20 are allowable.

CONCLUSION

In view of the foregoing, Applicant submits that claims 11-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are allowable, and that the application is in condition for allowance. Such action would be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below to discuss any other changes deemed necessary for allowance in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. The Commissioner is authorized to charge any deficiency in fees, including extension of time fees, or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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